

EAST - [10699890.wsp.1]

File View Edit Tools Window Help

Drafts
Pending
Active
L1: (14128) self-aligned adj contact\$1 or s
L2: (135) 1 and "DRAM" and (peripheral n
L3: (0) 2 and (gate and (sidewall near nitr
L4: (0) 2 and (gate and (sidewall near nitr
L5: (4) 2 and (gate and (sidewall near nitr
L6: (4) 2 and third near impurity
L7: (1) 2 and (third near impurity) and (co
Failed
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Favorites
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UDC
Queue
Trash

Browse Queue Clear

DBs: USPAT, EPO, JPO, DERWENT, IBM, TDB

Plurals

Default operator: OR

Highlight all hit terms initially

1 and "DRAM" and (peripheral near circuit)

BRST... ISAR... Image Text HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6748507 B2	20040608	71	Single-chip microcomputer with integral clock generating unit providing clock signals	711/167	709/209; 711/105;
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6744091 B1	20040601	93	Semiconductor storage device with self-aligned opening and method for	257/303	257/306
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6740550 B2	20040525	35	Methods of manufacturing semiconductor devices having chamfered silicide layers	438/199	438/592; 438/738;
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6735683 B2	20040511	71	Single-chip microcomputer with hierarchical internal bus structure having data and	712/1	710/100; 712/229;
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6731008 B1	20040504	25	Semiconductor device with conductive contact layer structure	257/774	257/296; 257/772;
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6727542 B2	20040427	18	Semiconductor memory device and method for manufacturing the same	257/306	257/303; 257/309
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6720606 B1	20040413	73	Dynamic semiconductor memory device having a trench capacitor	257/306	257/301
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6715028 B1	20040330	34	Data selecting memory device and selected data transfer device	711/104	365/189.05; 711/100;
9	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6710466 B2	20040323	25	Method of fabricating integrated circuit having self-aligned metal contact structure	257/758	438/233; 438/234
10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6706580 B2	20040316	26	Semiconductor memory of good retention and its manufacture	438/207	257/E21.649; 257/E21.659;
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6693002 B2	20040217	39	Semiconductor device and its manufacture	438/238	257/296; 257/303;